

IN THE CLAIMS

1-21. (Cancelled)

22. (Currently amended) A semiconductor device, comprising:
a semiconductor substrate having a low voltage region and a high voltage region;
a first isolation layer formed in the low voltage region and defining a first active region;
a second isolation layer formed in the high voltage region and defining a second active region;
a low voltage gate insulation layer formed on the first active region; and
a high voltage gate insulation layer formed on the second active region and having a greater thickness than the low voltage gate insulation layer, wherein a top surface of the second isolation layer is higher than that of the high voltage gate insulation layer, a step region between the high voltage gate insulation layer and the second isolation layer has no recessed region, and wherein a bottom portion of the step region is spaced apart from a vertical axis passing through an edge corner of the second active region toward the second isolation layer adjacent to the vertical axis.

23. (Original) The semiconductor device of claim 22, further comprising:
a low voltage gate electrode formed on the low voltage gate insulation layer, the low voltage gate electrode crossing over the first active region; and
a high voltage gate electrode formed on the high voltage gate insulation layer, the high voltage gate electrode crossing over the second active region.

24. (Original) The semiconductor device of claim 22, wherein the low voltage region is a memory cell array region.

25. (Original) The semiconductor device of claim 24, wherein the low voltage gate insulation layer is a tunnel oxide layer.

26. (Previously presented) The semiconductor device of claim 22, further comprising:

a control gate electrode formed over the low voltage gate insulation layer, the control gate electrode crossing over the first active region;

a floating gate interposed between the control gate electrode and the low voltage gate insulation layer;

a main gate electrode formed on the high voltage gate insulation layer, the main gate electrode crossing over the second active region;

a dummy gate electrode stacked on the main gate electrode; and

an inter-gate dielectric layer interposed between the floating gate and the control gate.

27. (Original) The semiconductor device of claim 22 further comprising a thermal oxide layer interposed between the first isolation layer and the semiconductor substrate, and between the second isolation layer and the semiconductor substrate.

28. (Original) The semiconductor device of claim 22, wherein an edge region of the first isolation layer is lower than a top surface of the low voltage gate insulation layer.

29. (Currently amended) A semiconductor device comprising:

a semiconductor substrate having a low voltage region and a high voltage region;

a first trench region formed in the low voltage region to define a first active region having a top surface, the first active region having a protruded edge portion-surface, that extends above the top surface;

a first sloped region interposed between the first trench region and the first active region, the first sloped region having a first incline that is downwardly extended from the protruded edge surface of the first active region;

a second trench region formed in the high voltage region to define a second active region, the second active region having a relatively flat top surface;

a second sloped region interposed between the second active region and the second trench region, the second sloped region having a second incline that is downwardly extended from the edge corner of the second active region;

a first isolation layer filling the first trench region and covering the first incline;

a second isolation layer filling the second trench region and covering the second incline;

a low voltage gate insulation layer formed on the first active region, the low voltage gate insulation layer having a top surface lower than a top surface of the first isolation layer; and

a high voltage gate insulation layer formed on the second active region, the high voltage gate insulation layer having a flat top surface lower than a top surface of the second isolation layer and being thicker than the low voltage gate insulation layer, the top surfaces of the low voltage gate insulation layer and the high voltage gate insulation layer having a profile without any recessed regions.

30. (Currently amended) The semiconductor device of claim 29, wherein the low voltage gate insulation layer on the protruded edge surface of the first active region is thinner than the low voltage gate insulation layer on ~~the~~ a central region of the first active region.

31. (Original) The semiconductor device of claim 29, wherein a vertical axis passing through the edge of the top surface of the low voltage gate insulation layer is located in the first sloped region.

32. (Previously presented) The semiconductor device of claim 33, wherein a distance between an upper corner of the first trench region and a lower corner of the low voltage gate electrode is greater than the thickness of the low voltage gate insulation layer.

33. (Original) The semiconductor device of claim 29, further comprising:
a low voltage gate electrode formed on the low voltage gate insulation layer and disposed to cross over the first active region; and
a high voltage gate electrode formed on the high voltage gate insulation layer and disposed to cross over the second active region.

34. (Original) The semiconductor device of claim 29, wherein the low voltage region is a memory cell region.

35. (Original) The semiconductor device of claim 34, wherein the low voltage gate insulation layer is a tunnel oxide layer.

36. (Original) The semiconductor device of claim 35, further comprising:

a control gate electrode formed over the tunnel oxide layer and disposed to cross over the first active region;

a floating gate interposed between the control gate electrode and the tunnel oxide layer;

an inter-gate dielectric layer interposed between the floating gate and the control gate electrode;

a main gate electrode formed on the high voltage gate insulation layer and disposed to cross over the second active region; and

a dummy gate electrode stacked on the main gate electrode.

37. (New) The semiconductor device of claim 22, wherein substantially the entire step region is spaced apart from the vertical axis passing through the edge corner of the second active region toward the second isolation layer adjacent to the vertical axis.

38. (New) The semiconductor device of claim 22, wherein a distance between the bottom portion of the step region and the bottom portion of an adjacent step region that is across the second active region is greater than the width of the top surface of the second active region.